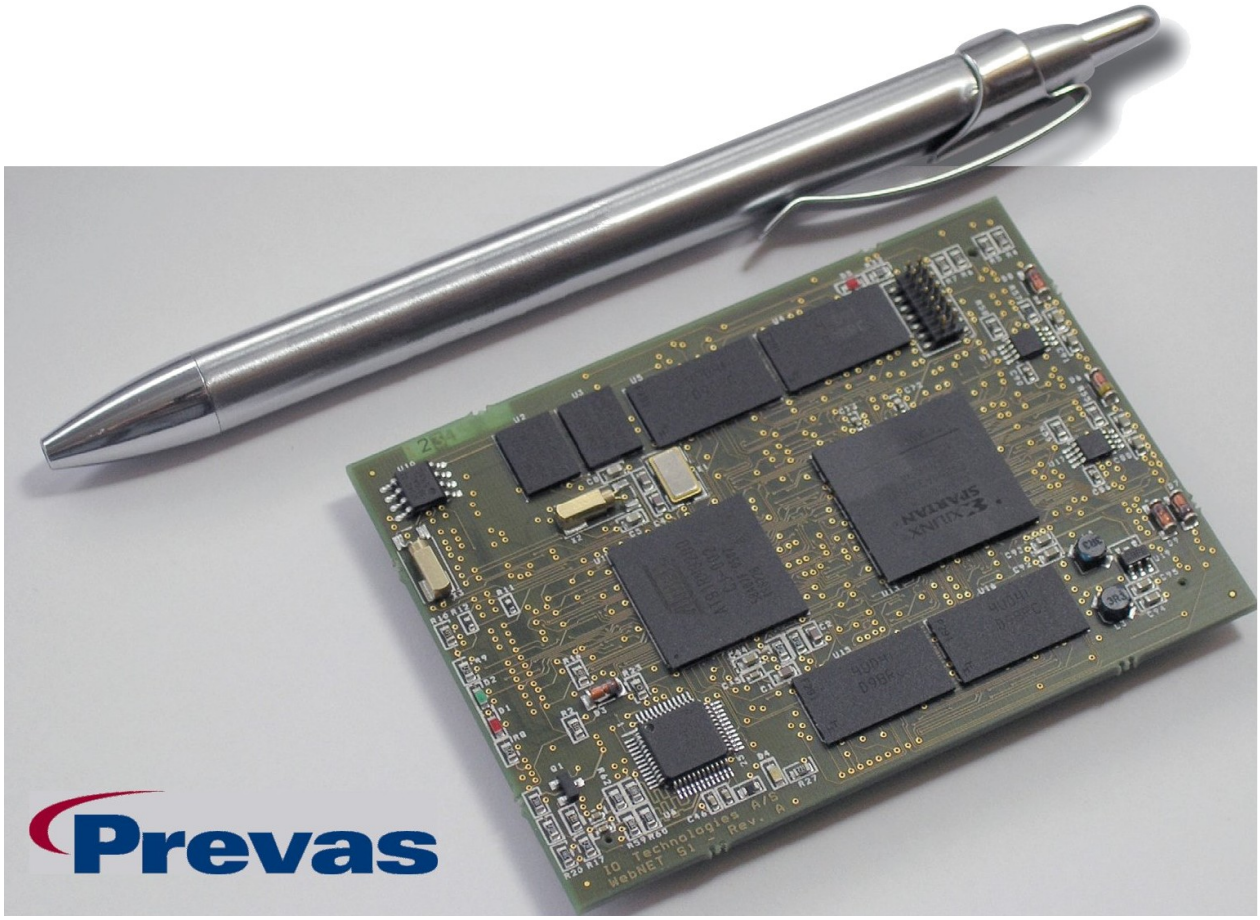
Prevas

WebNet S-1 Module

Powerful CPU with FPGA Co-processor



Data sheet

Introduction

The WebNet S-1 module contains an integrated CPU & Co-Processor with flexibility regarding interfaces and applications. E.g. it can have an Internet interface module and serve as Web Server. It contains a complete 32-bit ARM9 CPU system, based on AT91RM9200 from Atmel together with a FPGA SPARTAN 3E from Xilinx.
ARM9 CPU has up to 256 MB RAM, 32 MB FLASH and the FPGA is scalable from 250k gates to 1200k gates. The FPGA is connected to SDRAM with a size of 0-256 MB.

The S-1 module has a wide range of interfaces including twisted pair 10/100 Mbps Ethernet interface, USB host, USB device, serial ports and a series of GPIO's connected to both CPU and FPGA. The module is flexible and easy to customize by using the included development tools.

The total size of this module is only 75 mm × 55 mm

Module Feature Overview

The key hardware features are:

- 180 MHz ARM9 CPU with SDRAM and FLASH memory
- 180 MHz FPGA with 256 MB SDRAM
- 10/100 Mbps Ethernet interface
- 3 UARTs
- USB 2.0 host interface (full speed)
- USB 2.0 device interface (full speed)
- 32 CPU GPIOs with interrupt capability
- 64 FPGA GPIOs
- I2C (Inter-Integrated Circuit) bus
- Serial debug port (RS232)
- Watchdog and power-monitoring facility.
- Real Time Clock with support for battery backup
- High-speed interface through the FPGA for supporting various external units, including DSP's and video-displays.
- Programmable PLL clocks (up to 166MHz)
- Flexible TFT/LCD interface through FPGA
- 300MB/s video-memory bandwidth
- Single Supply: 3.3V, 2 Watt
- Size 75 mm × 55 mm
- Available at industrial temperature range: -40° - 85°C

SW parts:

- Complete Linux OS with http and ftp server.
- Open source development tools.

Some available FPGA features:

- SPI
- I2C
- Extra UARTs
- TFT/LCD Display controller
- Pulse-width modulation (PWM)
- Co-processor for CPU

System description

Multi Processor System.

The WebNet S-1 module contains three processors, ARM9 CPU, Spartan FPGA and an independent microcontroller for advanced system monitoring watchdog etc. Block diagram of the module core is shown in Figure 1. The module comes with a wide mix of memory sizes for both CPU and FPGA.

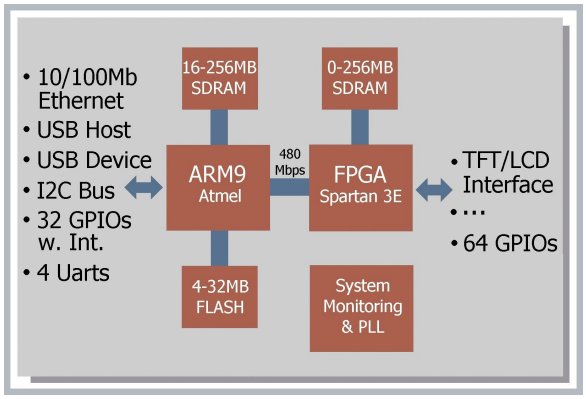


Figure 1 – WebNet S-1 Processor system

- 200 MIPS ARM9, Ethernet 10/100, Web server and USB 2.0. TFT/LCD interface through FPGA.
- 180 MHz FPGA with 256MB SDRAM and 64 parallel 100 MHz GPIOs.
- Independent µController (watchdog etc.) for advanced system monitoring.
- CPU FLASH memory scalable from 4-32 MB
- CPU SDRAM memory scalable from 16-256 MB
- FPGA SDRAM memory scalable from 0-256 MB

The ARM9 and FPGA can be configured to work either in serial or parallel computing. By default the ARM9 runs a Linux operating system which ensures a powerful embedded computer for man-machine interfaces and machine-machine network communication and surveillance. But other OS like ThreadX, Vx-Works, and Windows CE are also possible. The programmable FPGA is a true real-time data processor and may serve many purposes: DSP, flexible display interface, high-speed parallel I/O control, custom interface gateway. Figure 2 below shows the different layers in the ARM9 and the FPGA. The bus between the CPU and FPGA is running at 60 MHz (16bits, 1 wait state) and this gives a bandwidth of 480 Mbps.

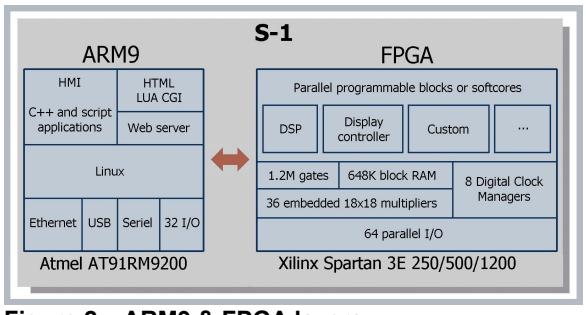


Figure 2 – ARM9 & FPGA layers

ARM processor, AT91RM9200 CPU

The ARM used is the AT91RM9200 LFBGA-256 from Atmel. It's a 200 MIPS processor @ 180Mhz with 16KByte data cache and 16Kbyte instruction cache. In normal mode it has a power consumption of 81 mW and 1,8mW in standby mode.
Address, data, and bus control signals are not available at the module connector.

The SDRAM for the ARM processor is selectable from 16 MB to 256 MB(2 memory banks), in either a 16 or 32 bit configuration.

The flash size is selectable from 4 MB to 32 MB where 2 chips are used. Flash retention time is 20 years or minimum 100.000 times/page.

FPGA: Spartan 3E

The FPGA used is the Xilinx Spartan 3E 250/500/1200 from Xilinx which is scalable from 250k gates to 1200k gates. The FPGA makes it fast and flexible to setup interfaces like e.g. TFT/LCD, SPI, I^2C, extra UARTs and custom bridging functionality. The FPGA is also powerful for implementing efficiently DSP solutions/algorithms e.g. filters and codecs for communication or image applications. And the FPGA can be used as a High Speed interface for supporting various external units including DSP's and video displays.

The SDRAM for the FPGA is selectable from 0 MB to 256 MB (2 memory banks).

The FPGA is connected directly to the address and data bus of the ARM9. This gives a high flexibility for FPGA usage and a high data transmission speed to between FPGA and ARM9.

Watchdog

For watchdog and power monitoring an ATmega88 (AVR) is used. This AVR processor handles power surveillance, power up sequence, and advanced debug facilities in case of errors. The AVR is able to generate a reset upon one or more of these events. The AVR processor can implement an intelligent watch dog able to determine the case and cause of a reset or power fail.
This AVR information can be programmed to be read out on the JTAG interface and give the user useful information in case of error or system generated reset.

The watchdog in details:

- The module provides a watchdog facility.
- Time-outs can be configurable from 1 second to 10 minutes.
- The watchdog is operational without any software intervention from the CPU after power-up.
- The watchdog is controlled from the CPU using a simple SPI interface.
- The ARM processor activity is checked through messages on the SPI interface at regular intervals. In case AVR-CPU messaging malfunction a reset will occur.
- The watchdog is able to reset the entire system, including units external to the WebNet S-1 module.

Programmable PLL clocks

The module has a programmable PLL (Phase Locked Loop) which can be used by the FPGA for applications that needs a custom frequency. This PLL is a CY22150 from Cypress which is capable to simultaneously generate several different output frequencies up to 166 MHz.

Debug features

The module provides facilities for debugging of CPU, FPGA code, and software on several levels. This ensures fast debugging of applications.

Initially user/costumer applications are normally developed on a host platform like PC, and here most functionality can be verified and debugged. On the host platform it is possible to set breakpoints and single step through the code. When applications seem to be running successful on the host it's time to check the application in target.

Target debugging are done by using a *telnet/ssh* connection from host to target platform. Through this interface command messages can be sent to the target and messages from the application can be watched. Also *Insight*, the advanced debugging utility, can be used for application debugging in target. This includes the possibility to set breakpoints and single step application execution.

Interpretation of messages from the Linux OS that is running on the ARM is useful for applications debugging. And a set of LED's are available for application usage/debugging.

Low level debugging is available:

- Serial RS232 debug port for ARM debugging and Linux kernel messages.
- JTAG interface for the FPGA.
- A set of LED's for the CPU debugging.
- JTAG interface for the CPU available on test points.

The primary debugging channel for the FPGA will be the JTAG interface.

The module contains LEDs for status indication. One of the LED's indicates that system is booting while another is used for indication of activity on the ARM processor. One LED is indicating if AVR is about to reset system. All LEDs are useful for getting an initial system status.

STANDARD INTERFACES

The section describes in more details the standard interfaces that are a part of the module,

Ethernet

The module comprises Ethernet interface on the board connector. The Ethernet is available from the ARM processor through the 10/100 Mbps PHY. All relevant hardware is on board the WebNet S-1 module except transformers and the physical RJ-45 connector. These must be placed on the main board. It is important to place the actual RJ45 connector as close to the WebNet S-1 module as possible and to keep tracks as short as possible. The Ethernet PHY LED signals are available on the S-1 connector. The Ethernet PHY used is the DP83848IW from National Semiconductors. It supports auto speed detection (10/100 Mbps). Operating range is up to 150 meters.

UARTs / RS232 / RS485

The WebNet S-1 module comprises 3 UARTs for general use and one for RS232 as a debug port. One of these general UARTs contains all modem control signals. These signals are Txd, Rxd, Cts, Dtr, Rts, Dsr, Dcd.
The remaining general UARTs contain hardware handshaking and hardware support for RS485 direction control.

The RS232 debug port has the Rxd and Txd signals on the S-1 connector and they are used to upload SW and debug low level code in the ARM processor.

The 3 general UARTs (RS232/RS485) are connected directly from the ARM processor - level driver and ESD protection must be placed on the main board.

The electrical interface is 3,3V TTL.

General purpose input/output (GPIO)

The module comprises 32 CPU GPIOs and 64 FPGA GPIOs. The CPU GPIOs are individually controlled by the ARM processor SW with regards to direction and state. It is also possible to use a number of these CPU GPIO's for interrupting the CPU.
The 64 FPGA GPIOs direction and state are configured individually by the used FPGA program.

For the CPU GPIOs the electrical interface is 3,3V TTL level. The FPGA the GPIOs has support for 3,3V TTL output and a wide range of input levels.

The GPIOs are not protected by buffers on the module itself so in some situation it is recommended to add buffer drivers on the main board in order to protect the GPOs.

USB 2.0 - host interface

The module comprises a USB full speed (12 Mbps) host interfaces. All relevant hardware is on the WebNet S-1 module except for the USB connector. This must be placed on the main board. The main board must also provide the 5V for the USB connector.

Key features for the USB host are:

- Complies with USB V2.0 Full-speed and Low-speed specifications.
- Supports both Low-speed 1,5 Mbps and Full-speed 12 Mbps.
- Root Hub integrated with 2 downstream ports.
- Embedded USB V2.0 Full-speed transceivers.
- Operates as master on the USB bus.
- Supports power management.

USB 2.0 - device interface

The module comprises USB full speed (12Mbps) slave interfaces. All relevant hardware is on the module except for the USB connector. This must be placed on the main board.

Key features for the USB device are:

- Supports both Low-speed 1,5 Mbps and Full-speed 12 Mbps
- Embedded USB V2.0 Full-speed transceivers

I2C (IIC) interface

The module comprises a standard 2-wire interface (I2C) and is available on the S-1 connector. The bus is made up of one clock line and one data line with speed up to 400 Kbps (Fast mode) based on byte-orientated transfer format. The bus is configurable for baud rate, permitting the data rate to be adapted to a wide range of core clock frequencies.

Key features are:

- Compatible with standard 2-wire Serial memory.
- 1 to 3 bytes of slave address.
- Sequential read / write operations.

Real time clock

The ARM processor contains a Real time Clock (RTC). It combines a time clock with an alarm function and a 200 year Gregorian calendar. Time and calendar values are coded in BCD format, and can run 12 and 24 hours mode.

The real time clock can be powered by an external battery on the main board

Key features are.:

- Low power consumption.
- 200 year calendar.
- Programmable periodic interrupt.

Power supply

The WebNet S-1 module requires a 3,3 VDC ±5% and is using approx 400mA @ 3,3 VDC.
This includes 225mA for the USB host interface.

The module provides the main board with the logical display signals, which the main board then converts into electrical formats required by the physical display

HIGH SPEED INTERFACE

The module provides a possibility to implement generic high-speed interfaces for customer specific main boards. The module provides a set of pins, which will be freely configurable by using the onboard FPGA. It is possible to use the pins to implement various interfaces. The high bandwidth of 480 Mbps between the CPU and FPGA ensures the possibility for high speed I/O to external units.

The following sections describe various use cases for the high speed interface.

TFT/LCD interface

By using the FPGA it is possible to interface to a TFT/LCD panel. The FPGA have access to up to 256 MB SDRAM which can be used for video buffer. And the throughput from this video buffer can be up to 300 MB/s. This interface will be connected to the TFT/LCD panel through connectors on the main board due to different connectors and electrical requirements for the broad range of displays.

High speed data collection

The FPGA can be used to sample data at a high speed. For storage of the samples the FPGA can use the SDRAM which have a size up to 256 Mb.

DSP connection

The FPGA also makes S-1 suitable for connecting a DSP to the module. Then the FPGA can be used for making a custom specific I/O with optional capability of processing to the DSP.

SOFTWARE OVERVIEW

This section gives a brief overview of the software Prevas supplies with the module. Both of the SW included on the S-1 module itself and the SW tools for host PC that is useful for S-1 SW development.

WebNet S-1 SW

The module comes with a complete Linux operating system. It' s based on a recent Linux kernel release. In February 2007 the module is supplied with kernel version 2.6.19 and includes all the drivers distributed with this kernel from www.kernel.org

The module has device-drivers for the peripherals described in this document and in addition to this, a set of standard applications are included e.g. system shell (ash), an AVR/FPGA loader, and various file and communication utilities.

The module comes with a standard firmware for the AVR controller and for the FPGA that makes it easy to take the module into use.

During boot the system is by default starting a range of services like loading FPGA image, GPIO driver and setting up Ethernet interface. The system also starts telnet, FTP (VSFTPD) and Web Servers (BOA).

This complete SW package on the WebNet S-1 makes the module easy to take into use and to perform costumer specific development on.

S-1 Peripheral interface drivers

The following lists some of the drivers that are included with the sw package:

- TTY driver for RS232 and RS45 ports.
- USB host driver with support for memory sticks, USB printer, USB mouse and much more.
- USB device driver with support for serial gadget (emulation of USB-to-serial which can be used in both Windows and Linux).
- Ethernet driver and kernel support for IPv4 and IPv6.
- I2C driver for easy access to the I2C bus from a C user space application.
- GPIO and OPB_GPIO driver for controlling the CPU and FPGA GPIOS from LUA script and C++.
- JFFS2 driver for journaling flash file system support.

S-1 Module applications

The following lists some of the applications included in the sw package.

- Linux Kernel with ARM patches
  The Linux Kernel with patches so it supports ARM processor based machines.
- AVR watchdog firmware
- BOA Web Server
  BOA is an open source tiny Web Server that offers extremely high performance specifically designed to run on Linux and suitable for embedded applications.
- Dropbear SSH server
  SSH (Secure Shell) is a set of standards and an associated network protocol that allows establishing a secure channel between a local and a remote computer. Dropbear is a open source relatively small SSH server and client. Dropbear SSH is particularly useful for "embedded"-type Linux systems.
- VSFTPD FTP server
  VSFTPD is an open source FTP server which is secure and extremely fast. VSFTPD (Very Secure FTP Daemon) is stable and supports IPv6 and SSL.
- Busybox unix tool box
  BusyBox is a software application which provides many standard Unix/Linux tools. BusyBox is designed to be a small executable for use with embedded Linux devices.
- Luacheia LUA distribution
  LUA is a script programming language that prides itself on ANSI C portability, small size, simplicity and ease of embedding. The LuaCheia LUA aim to make a full-featured programming language based on LUA that makes it more usable as a stand-alone language.
- Nano-X window system
  Nano-X Window System is an Open Source project aimed at bringing the features of modern graphical windowing environments to smaller devices and platforms. Nano-X allows applications to be built and tested on the Linux desktop, as well as cross-compiled for the target device.
- lrzsz X/Y/Z modem utilities
  lrzsz is an open source Unix/Linux communication package providing the XMODEM, YMODEM ZMODEM file transfer protocols.
- Netcat network utility
  Netcat is a network utility for reading from and writing to network connections on either TCP or UDP. It is designed in a thin and simple way, which makes it easy to incorporate in larger applications.
- PPP protocol
  Point-to-Point Protocol (PPP) is commonly used to act as a data link layer protocol for connection over synchronous and asynchronous connection between two nodes.
- Sudo user control system
  Sudo is a program for Unix/Linux that allows users to run programs with the security privileges of another user (normally the system's superuser) in a secure manner.
- Telser terminal program
  Telser is a serial port communication program
- Butler program
  for controlling the external watchdog, battery backed up Real time Clock (RTC), and temperature sensor.
- GDBserver debugger
  GNU debugger Server for remote debugging of the S-1 embedded Linux target. With this server debugging can be done from host PC and a range of debugging features is available. E.g. stop program execution on specified conditions,

examine what has happened when your program stopped.

S-1 specific commands

gpio	Sets/reads value of CPU GPIO.
avrdude	AVR content Downloader/UploaDEr
fpgamem	Writes/reads FPGAs address space
reboot	Reboots the module.
moduleconf	Shows the module configuration incl. network parameters.

SW development on PC (host)

The delivery from Prevas includes a range of tools for developing user applications for the WebNet S-1 module on a host PC. This section will give an overview of the tools and development process for making SW development for S-1 on a host PC.

Doing the development and testing on a host PC makes it fast to do the development for the S-1 module.

PC OS for WebNet S1 code development
SW developing is easy to do on host PC and then download to S-1 when needed. Since the S-1 platform is using a Linux kernel it is useful to have a Linux OS on the S-1 SW development PC. This can either be obtained by having a PC with a pure Linux OS installed or it can be obtained by running a virtual Linux machine on a Windows based PC. Prevas has instructions and SW image available for getting this virtual Linux machine up and running fast on a Windows PC. Prevas recommend using the user friendly Ubuntu Linux OS distribution which can be found at www.ubuntu.com.

WebNet S-1 code development
For developing SW for the S-1 on host several tools like compiler, linker, and libraries are needed on the host. All tools needed for development are already pre-installed on the virtual Linux machine image that is available from Prevas.

So after a fast session with host PC setup it is possible to start making and compiling programs on the host for the S-1 module. When the code has been written on the host PC it is cross-compiled for the S-1 ARM9 with Linux OS and transferred to S-1 module where it is executed and debugged if needed.

In some cases it makes sense first to compile it for the host PC and execute the code and debug it on the host PC before it is tried out on the S-1. This makes it possible to use all kinds of PC tools for testing and debugging.

Webpage development for WebNet S-1
The web pages for the S-1 Web Server can also be made, tested and debugged on the host platform. The web pages can be made as normal html pages (with some limitations to advanced html features) by using your favorite web page creator tool.

The S-1 web pages can also be made with LUA scripts. The LUA interpreter is included both in the S-1 module SW and with the Linux image for the PC development host.

LUA scripting provides a fast way to implement, test, debug, modify, and maintain Web Server directly on the WebNet S-1 module only by use of a Telnet or serial connection to the module. Or the LUA scripts has been made and tested on the host PC before they are transferred to the S-1 module without any need for compilation.

Since the LUA script is easy to read and there is no need for compilation. The scripts can be made or modified even on the S-1 module only by use of a Telnet or serial connection to the WebNet S-1 module.

For more details on LUA check www.lua.org

ARM SW development framework
Larger SW projects often benefits from using the software framework that is a part of an Integrated Development Platform. For making ARM applications the *Eclipse* platform can be used. Eclipse is an open source platform-independent software framework. There is a lot of Integrated Development Environments (IDE) available for the Eclipse platform which makes it easy to program in a wide range of programming languages like e.g. C/C++, Java, Photran, PHP, Python, Perl, Ruby, LUA, TCL, and COBOL.

Eclipse is not included with the SW deliveries from Prevas but is available from www.eclipse.org

FPGA code development
The FPGA code development is done on the host PC before it is transferred to the WebNet S-1. The ARM is loading the new code to the FPGA and it is taken into use.

The FPGA code is developed by using the FPGA code design tools from Xilinx which have several different design tools available depending on the functionality that is needed in the FPGA. More info on the FPGA code development can be found at
www.xilinx.com

The S-1 module comes with a default FPGA program that can be used for some applications.

Remote S-1 module debugger
The S-1 module includes a GDB (GNU Debugger) server which makes it possible to debug the S-1 module SW remotely from a host PC. This makes it possible to break code execution, set breakpoints, check stack and memory content of the S-1 module from the debugger on the host PC.

For the host PC several GUI's are available for this remote debugging. Prevas recommend using the Insight GUI which offers all standard features of a modern debugger and it has an easy-to-use graphical user interface and it supports application and system debugging over Ethernet or serial line.

More info on debugging with GDB and Insight can be found at the homepage sourceware.org/insight

CONNECTORS

The external connectors consist of two parts, the one part contains standard interfaces, including power signals and the other part contains a generic interface to the FPGA on the module.

Table 1 below shows the pin description for connector named “left side” on the footprint for the main board located in figure 3.

Pin	IO Name	Type	Function	Remarks
1	MAIN_BOARD_ID0	IO	GPIO	GPIO reserved for main board identification. Prevas will provide information of what ID to use.
2	UART5(TXD1)	IO		
3	MAIN_BOARD_ID1	IO	GPIO	
4	UART6(RXD1)	IO		
5	MAIN_BOARD_ID2	IO	GPIO	
6	UART9(CTS1)	IO		
7	MAIN_BOARD_ID3	IO	GPIO	
8	UART11(RTS1)	IO		
9	GND			
10	GND			
11	MAIN_BOARD_ID4	IO	GPIO	
12	UART4(DTR1)	IO		
13	MAIN_BOARD_ID5	IO	GPIO	
14	UART7(SCK1)	IO		
15	MAIN_BOARD_ID6	IO	GPIO	
16	UART8(DCD1)	IO		
17	MAIN_BOARD_ID7	IO	GPIO	
18	UART10(DSR1)	IO		
19	GND			
20	GND			
21	UART12(TXD3)	IO		
22	UART0(TXD0)	IO		
23	UART13(RXD3)	IO		
24	UART1(RXD0)	IO		
25	UART15(CTS3)	IO		
26	UART2(CTS0)	IO		
27	UART14(RTS3)	IO		
28	UART3(RTS0)	IO		
29	GND			
30	GND			
31	I2C0(TWD)	IO		
32	UART16(TXD_D)	IO		Debug Port
33	I2C1(TWCK)	IO		
34	UART17(RXD_D)	IO		Debug Port
35	CPU_IO0	IO	GPIO	
36	CPU_IO14	IO	GPIO	
37	CPU_IO1	IO	GPIO	
38	CPU_IO15	IO	GPIO	
39	GND			
40	GND			
41	CPU_IO2	IO	GPIO	
42	CPU_IO16	IO	GPIO	
43	CPU_IO3	IO	GPIO	
44	CPU_IO17	IO	GPIO	
45	CPU_IO4	IO	GPIO	
46	CPU_IO18	IO	GPIO	
47	CPU_IO5	IO	GPIO	
48	CPU_IO19	IO	GPIO	
49	GND			
50	GND			
51	CPU_IO6	IO	GPIO	
52	CPU_IO20	IO	GPIO	
53	CPU_IO7	IO	GPIO	
54	CPU_IO21	IO	GPIO	
55	CPU_IO8	IO	GPIO	
56	CPU_IO22	IO	GPIO	
57	CPU_IO9	IO	GPIO	
58	CPU_IO23	IO	GPIO	
59	GND			
60	GND			
61	CPU_IO10	IO	GPIO	
62	CPU_IO24	IO	GPIO	
63	CPU_IO11	IO	GPIO	
64	CPU_IO25	IO	GPIO	
65	CPU_IO12	IO	GPIO	
66	CPU_IO26	IO	GPIO	
67	CPU_IO13	IO	GPIO	
68	CPU_IO27	IO	GPIO	
69	AVR_IO0	IO		
70	EXT_PWR_SURVAILANCE0	IO	PWR_FAIL	External power fails
71	AVR_IO1	IO		
72	EXT_PWR_SURVAILANCE1	IO	PWR_FAIL	External power fails
73	GND			
74	GND			
75	PLL_CLK1	O		
76	ARM_MAN_PROTECT	IO		
77	PLL_CLK2	O		
78	RTC_BATT	I		
79	3V3			
80	3V3			
81	3V3			
82	3V3			
83	3V3			
84	3V3			
85	ETHERNET2 COL	IO		
86	EXT_RESET1	I		
87	ETHERNET0 LINK	IO		
88	EXT_RESET0	I		
89	ETHERNET1 SPEED	IO		
90	USB2 Device_CON	IO		
91	GND			
92	GND			
93	ETHERNET3 TD+	IO		
94	USB1 Device_P	IO		
95	ETHERNET4 TD-	IO		
96	USB0 Device_M	IO		
97	ETHERNET5 RD+	IO		
98	USB4 HOST_P	IO		
99	ETHERNET6 RD-	IO		
100	USB3 HOST M	IO		

Table 1 Pin description for “left side” connector.

Table 2 below shows the pin description for connector named “right side” on the footprint for the main board located in figure 3.

Pin	IO Name	Type	Function	Remarks
1	FPGA_IO0	IO	GPIO	
2	FPGA_IO32	IO	GPIO	
3	GND			
4	GND			
5	FPGA_IO1	IO	GPIO	
6	FPGA_IO33	IO	GPIO	
7	FPGA_IO2	IO	GPIO	
8	FPGA_IO34	IO	GPIO	
9	GND			
10	GND			
11	FPGA_IO3	IO	GPIO	
12	FPGA_IO35	IO	GPIO	
13	FPGA_IO4	IO	GPIO	
14	FPGA_IO36	IO	GPIO	
15	GND			
16	GND			
17	FPGA_IO5	IO	GPIO	
18	FPGA_IO37	IO	GPIO	
19	FPGA_IO6	IO	GPIO	
20	FPGA_IO38	IO	GPIO	
21	GND			
22	GND			
23	FPGA_IO7	IO	GPIO	
24	FPGA_IO39	IO	GPIO	
25	FPGA_IO8	IO	GPIO	
26	FPGA_IO40	IO	GPIO	
27	FPGA_IO9	IO	GPIO	
28	FPGA_IO41	IO	GPIO	
29	GND			
30	GND			
31	FPGA_IO10	IO	GPIO	
32	FPGA_IO42	IO	GPIO	
33	FPGA_IO11	IO	GPIO	
34	FPGA_IO43	IO	GPIO	
35	FPGA_IO12	IO	GPIO	
36	FPGA_IO44	IO	GPIO	
37	FPGA_IO13	IO	GPIO	
38	FPGA_IO45	IO	GPIO	
39	GND			
40	GND			
41	FPGA_IO14	IO	GPIO	
42	FPGA_IO46	IO	GPIO	
43	FPGA_IO15	IO	GPIO	
44	FPGA_IO47	IO	GPIO	
45	FPGA_IO16	IO	GPIO	
46	FPGA_IO48	IO	GPIO	
47	FPGA_I17	IO	GPIO	
48	FPGA_IO49	IO	GPIO	
49	GND			
50	GND			
51	FPGA_IO18	IO	GPIO	
52	FPGA_IO50	IO	GPIO	
53	FPGA_IO19	IO	GPIO	
54	FPGA_IO51	IO	GPIO	
55	FPGA_IO20	IO	GPIO	
56	FPGA_IO52	IO	GPIO	
57	FPGA_IO21	IO	GPIO	
58	FPGA_IO53	IO	GPIO	
59	GND			
60	GND			
61	FPGA_IO22	IO	GPIO	
62	FPGA_IO54	IO	GPIO	
63	FPGA_IO23	IO	GPIO	
64	FPGA_IO55	IO	GPIO	
65	FPGA_IO24	IO	GPIO	
66	FPGA_IO56	IO	GPIO	
67	FPGA_IO25	IO	GPIO	
68	FPGA_IO57	IO	GPIO	
69	GND			
70	GND			
71	FPGA_IO26	IO	GPIO	
72	FPGA_IO58	IO	GPIO	
73	FPGA_IO27	IO	GPIO	
74	FPGA_IO59	IO	GPIO	
75	FPGA_IO28	IO	GPIO	
76	FPGA_IO60	IO	GPIO	
77	FPGA_IO29	IO	GPIO	
78	FPGA_IO61	IO	GPIO	
79	GND			
80	GND			
81	FPGA_IO30	IO	GPIO	
82	FPGA_IO62	IO	GPIO	
83	FPGA_IO31	IO	GPIO	
84	FPGA_IO63	IO	GPIO	
85	GND			
86	GND			
87	CPU_IO28	IO	GPIO	
88	GND			
89	CPU_IO29	IO	GPIO	
90	FPGA_INPUT0	IO	GPIO	
91	CPU_IO30	IO	GPIO	
92	FPGA_INPUT1	I	GPIO	
93	GND			
94	GND			
95	CPU_I31	IO	GPIO	
96	FPGA_INPUT2	I	GPIO	
97	CPU_IO32	IO	GPIO	
98	FPGA_INPUT3	I	GPIO	
99	CPU_IO33	IO	GPIO	
100	FPGA_INPUT4	I	GPIO	

Table 2 Pin description for “right side” connector

MECHANICAL SPECIFICATION

The WebNet S-1 module is attached to the main board via two 100 pins connectors. The connectors located on the S-1 module are from Tyco Electronics with part number 5177983-4.

On the main board the connections to the WebNet S-1 are made with the connector from Tyco Electronics with part number 5177984-4. The connectors are available with several different heights which makes it possible to place components on the main board under the Webnet S-1 module. More info on this issue can be seen from the Tyco connector catalog.

Diagram symbol and PCB foot print are available from Prevas when they are needed for diagram drawing or PCB layout of main board.

Figure 3 shows the Foot print for PCB layout of the main board. It shows the size (in mm) of the S-1 PCB and the location of the connectors.

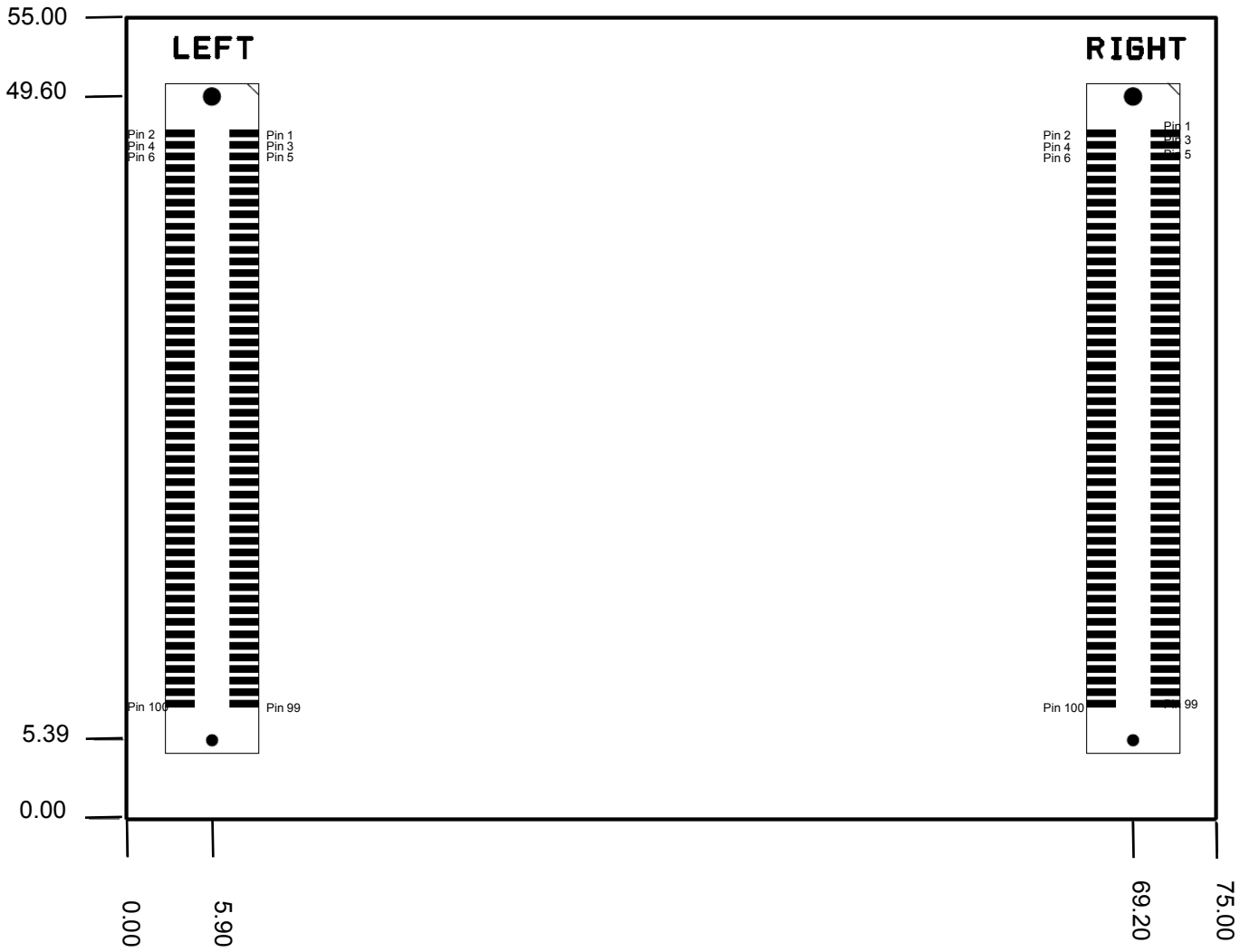


Figure 3 Foot print for PCB layout of the main board

ENVIRONMENTAL

The module will comply to industrial operating temperatuddre ratings, which is -40°C to +85°C and humidity rating from 0 to 95% non-condensing.

The module is tested for resistance to vibration.