SocEye – On Chip Monitoring System

- Hardware based black box monitoring

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Features

- Simplifies test and verification process
- Samples time stamped events from both software and hardware, based on system clock
- No probe effect in hardware and one instruction in software.
- 24 hours a day Monitoring
- Analyzes all levels of abstraction
- Easy to add custom plug-ins to the analysis tool
- Multiprocessor monitoring
- Powerful debugging tool
- Highly suitable for FPGA/ASIC/PCB designs
- RTOS and processor independent
- Supports user defined events and SW-probe events
- Handles 5000 events per second

Prevas SocEye monitoring system consists of:

- An on-chip black box
- A computer system analyzer
- A SQL database

A traditional monitoring system often includes a processor module for locating software problems, a bus analyzer for monitoring bus activity and a logic analyzer for isolating logic and timing problems in hardware. Prevas SocEye is however different since both hardware and software events could be monitored using the same device.

It is easy to implement the black box as an Intellectual Property-component (IP) in a System-on-Chip, overcoming the difficulties relative to probing obstructive hardware. Using Prevas SocEye substantially reduces a products development time and enables cost-effective monitoring. The SocEye system is extremely versatile; it can be used in numerous types of monitoring applications. A further advantage is that all data is time stamped and stored in a database and thus, very easy to analyze “off-line”.

On-Chip monitoring has also the advantage that it is speed independent, since the hardware part of the monitor uses the same frequency as the target system.

CORE Facts

Provided with Core	
Documentation	User’s Reference Manual
Design File Formats	HW: EDIF netlist; VHDL Source RTL (available at extra cost) SW: System Analyzer
Constraints Files	soceye.ucf
Verification	VHDL test bench
Instantiation templates	VHDL
Reference designs & application notes	HW/SW verification has been executed in Xilinx EDK 7.1i.
Additional Items	None
Simulation Tool Used	
ModelSim™ XE-III 6.0a	
Support	
Support provided by Prevas	

Supported Family	Device tested	CLB Slices	Clock IOBs	IOBs	Performance* (MHz)	Xilinx Tools
Virtex -4	XC4VLX25	274	1	107	152	ISE 7.1i
Virtex -II Pro	XC2VP20	274	1	107	128	ISE 7.1i
Spartan-3	XC3S400	277	1	107	77	ISE 7.1i

Table 1: Example Implementation Statistics

*Increases with more than 50 %, when optimizing for speed

Prevas SocEye IP core is technology, Real-Time Operating System (RTOS) and processor independent.

Typical Applications

- Testing and debugging applications
- Analyzing a target system crash
- Continuous process monitoring

Application

Prevas SocEye is suitable for all kinds of small and medium System-on-Chip. It is flexible and can be used for testing and debugging, continuous monitoring and it analyzes target system crashes, e.g. as a Black Box. Moreover, Prevas SocEye will simplify your system monitoring and design and shorten time to market. Prevas SocEye and can also be used as a Prevas Sierra Monitor.

Specifics

Prevas SocEye, supports software probe and user defined events. On request, Prevas SocEye can be extended to other configurations, e.g. more events, resources etc. Contact Prevas for more information.

Functional description

Prevas SocEye is partitioned into modules as shown in Figure 1 and described in the text below.

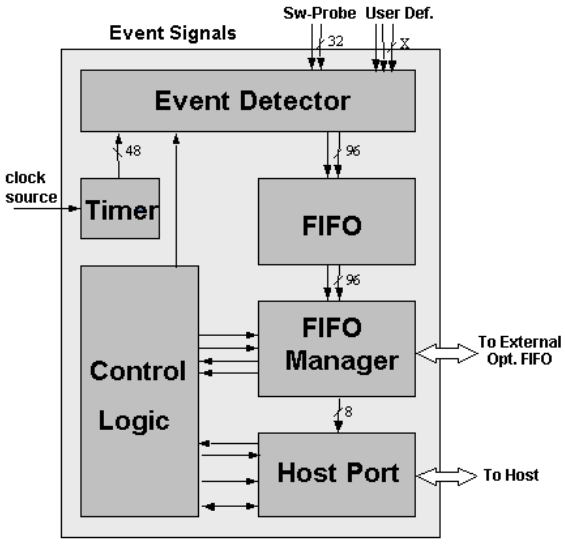

Figure 1 - Architecture of the SocEye Black Box

On-Chip black box

The hardware part (black box) is partitioned into functional units

- Event detector
- FIFO
- FIFO Manager
- Host Port, USB, EPP or Serial connection

Event Detector

The Event Detector is responsible for the detection of events and for collecting event samples. Over-sampling of the input signals is not required because the predefined events will never occur simultaneously. When an event is detected, a sample is collected and stored immediately along with a timestamp in the local FIFO buffer.

An event-sample comprises the event-type, the timestamp, and an event defined parameter field. The parameter field is used to store additional information about an event. For instance, for a software-probe event to be sufficiently informative, the parameter field contains current software-probe ID-number and a timestamp. A single strobe line is all that is required to indicate a software write-access, and to signal the hardware unit to latch incoming data.

The timestamp comes from the 48-bit Timer module, which denotes the absolute system time given in nanoseconds. The Timer is updated at the resolution of the system clock frequency.

FIFO

The FIFO buffer is used during transient over-loads of events while the host computer is busy reading event data over the host port. The FIFO is built onto on-chip dual ported RAM with parameterizable (generic) size and port width.

FIFO Manager

The FIFO Manager mainly provides a byte-wide interface for the Host Port to read event data from the FIFO. In circumstances when the required FIFO size is not feasible on-chip, e.g. in FPGA implementations, the FIFO Manager can also be used to extend the FIFO using external RAM. In this case, the FIFO Manager will also take care of flushing the contents of the on-chip FIFO out to the external RAM. The option to use external RAM can be set via the Host Port.

Host Port

The Host Port is responsible for taking care of host-initiated acquisition of event data. It also provides the host with a programming interface to read the status of the Black Box and to control its behaviour. Since FIFO buffering is limited it is important that event samples are transferred to the host with a guaranteed high communication bandwidth. The host port is configured to support one of the following communication protocols:

- Universal Serial Bus (USB)
- Enhanced Parallel Port (EPP)
- Serial Communication via UART

To indicate availability of events in the FIFO the Host Port can be programmed to generate an interrupt to the host computer. When this feature is enabled, it can be set into one of three modes:

- Interrupt whenever new events arrive
- Interrupt when the FIFO buffer is half-full
- Interrupt when the FIFO buffer is full

The first two modes are useful when continuous monitoring is desired. The third mode is more useful if the black box is set to sample from a given command until the FIFO becomes full, and then stops. Providing the ability to choose the interrupt mode gives a customised solution that best suits the capabilities of the host computer performance, the tools, or the user. When the interrupt function is disabled, events can still be acquired in polled mode.

Pinout

The hardware part signals are described below. The host port pins are dependent of communication method and is therefore generalized.

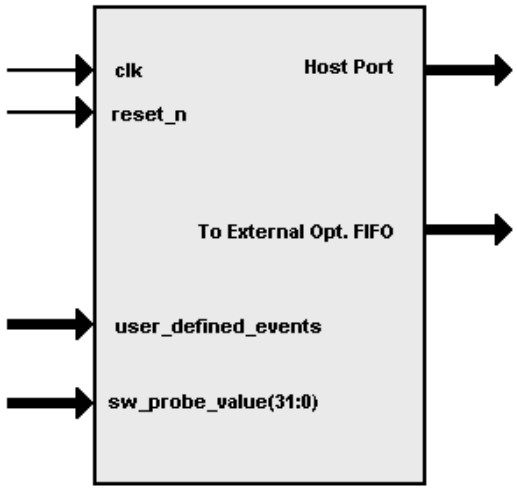

Figure 2: Basic Pinout Overview

Signal	Direction	Description
clk	IN	System clock
reset_n	IN	System reset
user_defined_events	IN	User predefined events
sw_probe_value	IN	SW-Probe Value
Host Port	OUT	Technology Dependent Ports (USB, EPP, Serial)
To External Opt. FIFO	OUT	To External FIFO

Table 2: PinOut

Host Computer System Analyzer

To provide the user with a platform for event-based performance analysis and debugging, a monitoring application is used. The application uses an SQL database to store the event histories. At the bottom lies the black box interface module, which is mainly used to transfer event samples from the black box into the SQL database, and to control the behaviour of the black box.

The application provides an integrated interface to control the monitoring process, to collect events into the database, and to query the event database in various ways. Using this interface makes it easy to implement application specific monitoring tools, which can be used for finding and analyzing erroneous execution patterns, collecting events from the database, and display them along a timeline. Apart from standard functions such as zooming and scrolling, there is also support for time-markers that are used for timing measurements, and search-markers that can be used to locate event conditions and patterns. The event database is also suitable for other post-analysis, such as;

- Extraction of performance indexes for use in diagrams
- Histograms showing execution times
- Processor utilisation
- Inter Process Communication (IPC) frequencies
- Interrupt response times

Verification Methods

Functional simulation of Prevas SocEye monitoring system was carried out using Model Technology ModelSim™ XE-III 6.0a.

The core has been verified and used in systems with Xilinx FPGAs, for cache analysis and for monitoring of RTOS.

Functional co-verification of Prevas SocEye hardware together with software has been executed in Xilinx EDK 7.1i.

Design Services

Prevas also offers core integration, core customisation and other design services.

Ordering Information

This product is available from Prevas, under terms of the SignOnce IP License. See www.prevas.se or contact Prevas for more information about this product.

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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